Design and Optimization of T-Coil-Enhanced ESD Circuit with Upsampling Convolutional Neural Network

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***Abstract*— T-coils are widely used in high-speed electrostatic discharge (ESD) circuits to increase bandwidth. Like many other RF/microwave devices, T-coil modeling relies on time-consuming electromagnetic (EM) simulations, which precludes quick design space exploration and fast global optimization. In this paper, a machine learning (ML) model is presented to replace EM T-coil simulations, thereby accelerating T-coil design and optimization. Given the geometry of a T-coil layout, the ML model can infer its S-parameters from 100 MHz to 100 GHz nearly instantly. Finally, this ML model is incorporated into a genetic algorithm (GA), affording a 10× speed improvement in the optimization of a T-coil-enhanced ESD circuit in a 22nm FD-SOI CMOS process.**

***Keywords*— electrostatic discharge (ESD), genetic algorithm (GA), machine learning (ML), T-coil.**

I. Introduction

A T-coil is a three-port device frequently employed to enhance the bandwidth of high-speed electrostatic discharge (ESD) circuits [1]. Figure 1a shows the model of a T-coil in an ESD circuit, and Figure 1b shows the layout of a T-coil, where L is the outer diameter, W is the metal width, N_{in} is the number of inner segments, and N_{out} is the number of outer segments. Due to the complexity of the circuit's response, usually many numerical analysis and repetitive computationally-expensive electromagnetic (EM) simulations would be required to find the best T-coil design [2].

In order to speed up T-coil design, we propose replacing the EM simulator with a machine learning (ML) model to predict the T-coil S-parameters, dramatically accelerating design iterations. In [3], a deconvolutional neural network was used to make the inductance and resistance predictions for off-chip inductors. However, the neural network topology suffered from the checkerboard artifact caused by the uneven overlapping during the deconvolution operations, which increased its prediction error [4]. This work addresses that shortcoming in the more complex case of a three-port integrated T-coil.

In this paper, an artifact-free model using an upsampling convolutional neural network (CNN) is proposed. The model is incorporated into a genetic algorithm (GA) to find a T-coil layout that satisfies a set of ESD circuit specifications while minimizing area. The final results show a 10× speed improvement compared to using traditional EM simulators, with reasonable accuracy of the proposed ML model.

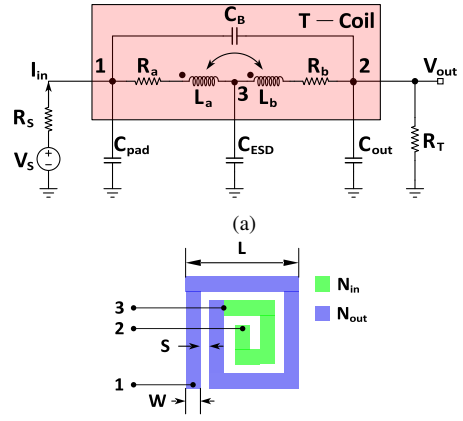


Fig. 1. (a) T-coil-enhanced ESD circuit; (b) simplified T-coil layout, where in this case N_{in} = 4 and N_{out} = 5.

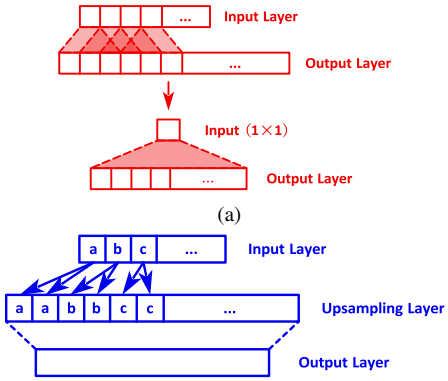


Fig. 2. (a) Overlapping during the deconvolutional operation, which can be removed by having a unity-size input; (b) upsampling convolutional layer, which consists of a pure upsampling layer and a CNN.

II. ML Model for EM Simulator Replacement

A. Upsampling Convolutional Neural Network

The EM replacement model in this work predicts the broadband S-parameters of a T-coil from its geometric parameters. Since the model must produce many more outputs (i.e., complex-valued S-parameters across a wide frequency range) than the inputs $(L, W, S, N_{in}, N_{out})$, upsampling is required. In [3] a deconvolutional neural network model was proposed for this purpose because it requires fewer trainable weights than alternative neural network topologies

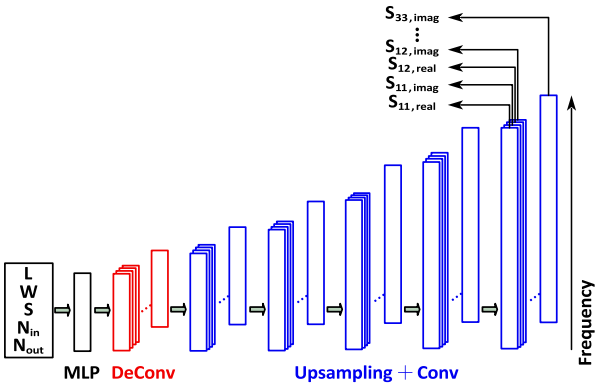


Fig. 3. The proposed ML model for predicting T-coil S-parameters.

such as the multi-layer perception (MLP) or CNN. However, as [4] discussed, uneven overlapping during the deconvolution operations will lead to the checkerboard artifact. This phenomenon is illustrated in Figure 2a, where the darker color regions overlap with more deconvolutions, and arises when the stride size is not an integer multiple of the output window.

As discussed in [5], it is possible to use upsampling convolutional layers to replace deconvolutional layers to avoid the checkerboard artifact. As shown in Figure 2b, the upsampling convolutional layer consists of a pure upsampling layer that uses the nearest-neighbor algorithm with an upsampling factor of 2, followed by a convolutional layer. However, it is noted that by doing so, more upsampling convolutional layers are required to replace the deconvolutional layers for the same output size, which requires more training and may carry a higher risk of overfitting. Alternatively, a single deconvolutional layer whose input size is only one is known to be artifact-free (Figure 2a). Therefore, we propose to use such a deconvolutional layer in conjunction with upsampling convolutional layers to compromise the number of trainable weights and mitigate the risk of overfitting.

Figure 3 shows the final ML model architecture. The first MLP section will map the input T-coil geometric parameters to some higher dimension abstract representations. It is followed by an artifact-free deconvolutional layer and a series of upsampling convolutional layers. The final outputs are the real and imaginary parts of S_{11}, S_{12}, S_{13}, S_{22}, S_{23}, and S_{33} from 100 MHz to 100 GHz with a frequency step size of 100 MHz.

B. Simulation Results

The loss function used to train and test the proposed model is a modified mean squared error, as in [3]:

$$L_{freq} = \frac{1}{N}\sum_{n=1}^{N}\sqrt{\frac{1}{K}\sum_{k=1}^{K}(S_{n,k} - \hat{S}_{n,k})^2} \qquad (1)$$

where N is the number of elements in the training set, K is the number of frequency points, $S_{n,k}$ is the true S-parameters (obtained by EM simulation) at frequency point k for the n^{th} T-coil, and $\hat{S}_{n,k}$ is the corresponding prediction. This loss function trains the model to minimize the error across all frequencies instead of only focusing on each individual frequency point. In this work, 2570 T-coil layouts in a 22nm FD-SOI CMOS process are EM-simulated with Cadence® EMX® from 100 MHz to 100 GHz, and 80% of these simulation results are used to train the ML model. It accepts five input T-coil geometric parameters $(L, W, S, N_{in}, N_{out})$ and predicts the corresponding S-parameters. The range of these five input T-coil geometric parameters are listed in Table 1.

Table 1. Design Parameters of T-Coil.

Parameter	Unit	Min	Max
Outer Diameter L	μm	32	80
Metal Width W	μm	2.4	5
Metal Spacing S	μm	1.2	1.44
Inner Segments N_{in}	-	5	25
Outer Segments N_{out}	-	4	12

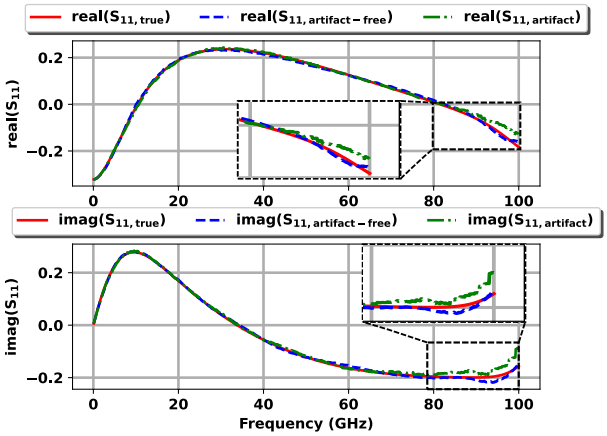
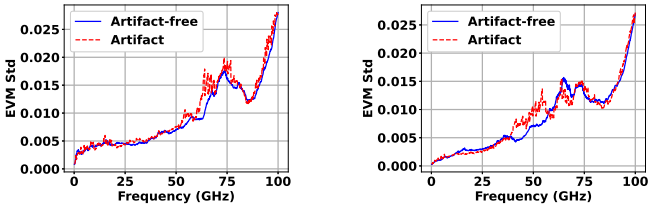


Fig. 4. S_{11} of a test case. The upper subplot is the real part of S_{11} and the lower subplot is the imaginary part of S_{11}.

In order to show how the checkerboard artifact manifests itself in the predicted S-parameters, the proposed ML model and the deconvolutional model from [3] are trained in 3000 epochs and tested, all on the same datasets as our artifact-free model. Figure 4 shows the resulting S_{11} of a test case. The checkerboard artifact can be seen more obviously in the inset at high frequencies. The standard deviation of the S-parameter error vector magnitude (EVM) across all 514 test cases is used to quantify the effect of the checkerboard artifact:

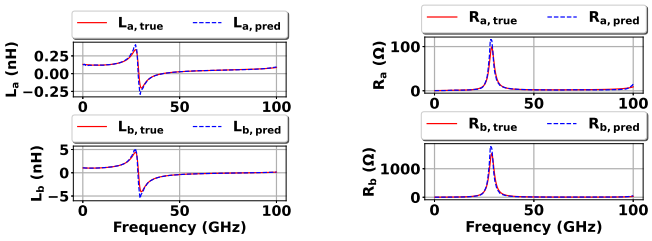
$$EVM_{n,k} = \sqrt{\left(S_{n,k} - \hat{S}_{n,k}\right)^2} \qquad (2)$$

where $EVM_{n,k}$ is the EVM of the S-parameters at the frequency point k for the n^{th} T-coil. From our 514 test cases, it is found that S_{11} and S_{13} are most impaired by the checkerboard artifact, as shown in Figure 5. The EVM standard deviation increases with frequency, and more fluctuations are observed for the deconvolutional model. Therefore, the proposed ML model provides smoother and more accurate results. Using the predicted S-parameters, the



(a) (b)

Fig. 5. (a) The standard deviation of EVM of S_{11}; (b) the standard deviation of EVM of S_{13}. Plots are generated from 514 test cases.



(a) (b)

Fig. 6. (a) Inductance of a test t-coil; (b) resistance of a test t-coil.

T-coil's inductance and resistance can be accurately inferred as well, as shown in Figure 6.

III. T-Coil-Enhanced ESD Circuit Optimization

A. Optimization Setup

The previously proposed ML model can replace EM simulators during T-coil-enhanced ESD circuit optimization. Two common metrics are used to evaluate the performance of the ESD circuit: its 3-dB transimpedance bandwidth $BW_{R_{tran}}$ where the transimpedance is $R_{tran} = V_{out}/I_{in}$ in Figure 1a, and -10 dB return loss bandwidth $BW_{S_{11}}$ [6]. For example, we configure a genetic optimization algorithm to find the smallest T-coil layout that makes both $BW_{R_{tran}}$ and $BW_{S_{11}}$ larger than 30 GHz and smaller than 40 GHz, while assuming C_{pad} = C_{ESD} = C_{out} = 100 fF and R_S = R_T = 50 Ω in Figure 1a. Ten GA generations are used, with 100 individuals in each generation.

B. Optimization Results

The whole optimization runs on an Intel® Xeon® Gold 6242R CPU, and it takes about 2 hours for the entire optimization to be completed without multiprocessing. The final T-coil layout geometric parameters are [L, W, S, N_{in}, N_{out}] = [32μm, 1.2μm, 1.44μm, 12, 9], and the area is the smallest that the T-coil parameterized cell (PCell) of this process technology can achieve, which is 1024 μm^2. Table 2 summarizes the final optimization results. By comparison, it will take approximately 20 hours if the Cadence® EMX® is used instead. Therefore, an approximate 10× speed improvement is achieved using the proposed ML model. Without the ML model, most computation time is spent on EM simulations. Using the ML model, the S-parameters are found almost instantly, so most of the computation time is spent on extracting an equivalent circuit model for the T-coil from its S-parameters and in Spice simulation of the ESD

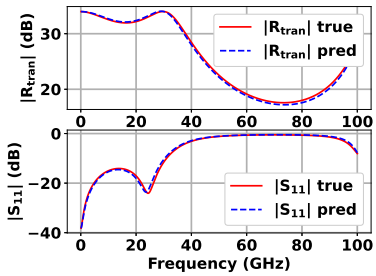


Fig. 7. Transimpedance $|R_{tran}|$ and return loss $|S_{11}|$ of the optimized T-coil-enhanced ESD circuit.

Table 2. T-Coil Optimization Results.

Model	**$BW_{R_{tran}}$ (GHz)**	**$BW_{S_{11}}$ (GHz)**	**Area (μm^2)**	**Normalized Runtime**
ML	36.6	30.8	1024	**1**
EMX	36.3	30.7	1024	**≈10**

circuit. In order to validate the accuracy of the final design, the optimal T-coil layout is further evaluated by the Cadence® EMX®, then used for ESD circuit simulations. The results are shown in Figure 7 where we see the ML model's predictions match the EM simulations very precisely.

IV. Conclusion

In this paper, an ML model is presented to replace EM simulators, rapidly predicting the broadband S-parameters of a T-coil. The proposed ML model is then used together with a GA to optimize a T-coil-enhanced ESD circuit. Final results show the accuracy of the proposed ML model and its potential to accelerate design.

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References

[1] B. Razavi, "The bridged t-coil [a circuit for all seasons]," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 4, pp. 9–13, 2015.

[2] M. Kossel, C. Menolfi, J. Weiss, P. Buchmann, G. von Bueren, L. Rodoni, T. Morf, T. Toifl, and M. Schmatz, "A t-coil-enhanced 8.5 gb/s high-swing sst transmitter in 65 nm bulk cmos with « -16 db return loss over 10 ghz bandwidth," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 12, pp. 2905–2920, 2008.

[3] H. M. Torun, H. Yu, N. Dasari, V. C. K. Chekuri, A. Singh, J. Kim, S. K. Lim, S. Mukhopadhyay, and M. Swaminathan, "A spectral convolutional net for co-optimization of integrated voltage regulators and embedded inductors," in *2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2019, pp. 1–8.

[4] A. Odena, V. Dumoulin, and C. Olah, "Deconvolution and checkerboard artifacts," *Distill*, 2016. [Online]. Available: http://distill.pub/2016/deconv-checkerboard

[5] W. Shi, J. Caballero, F. Huszár, J. Totz, A. P. Aitken, R. Bishop, D. Rueckert, and Z. Wang, "Real-time single image and video super-resolution using an efficient sub-pixel convolutional neural network," 2016.

[6] S. Galal and B. Razavi, "Broadband esd protection circuits in cmos technology," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 12, pp. 2334–2340, 2003.